Release 14.7 - xst P.20131013 (nt64)

Copyright (c) 1995-2013 Xilinx, Inc. All rights reserved.

--> Parameter TMPDIR set to xst/projnav.tmp

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.09 secs

--> Parameter xsthdpdir set to xst

Total REAL time to Xst completion: 0.00 secs

Total CPU time to Xst completion: 0.09 secs

--> Reading design: ALEY\_MULTIPLIER.prj

TABLE OF CONTENTS

1) Synthesis Options Summary

2) HDL Compilation

3) Design Hierarchy Analysis

4) HDL Analysis

5) HDL Synthesis

5.1) HDL Synthesis Report

6) Advanced HDL Synthesis

6.1) Advanced HDL Synthesis Report

7) Low Level Synthesis

8) Partition Report

9) Final Report

9.1) Device utilization summary

9.2) Partition Resource Summary

9.3) TIMING REPORT

=========================================================================

\* Synthesis Options Summary \*

=========================================================================

---- Source Parameters

Input File Name : "ALEY\_MULTIPLIER.prj"

Input Format : mixed

Ignore Synthesis Constraint File : NO

---- Target Parameters

Output File Name : "ALEY\_MULTIPLIER"

Output Format : NGC

Target Device : xc4vlx100-12-ff1148

---- Source Options

Top Module Name : ALEY\_MULTIPLIER

Automatic FSM Extraction : YES

FSM Encoding Algorithm : Auto

Safe Implementation : No

FSM Style : LUT

RAM Extraction : Yes

RAM Style : Auto

ROM Extraction : Yes

Mux Style : Auto

Decoder Extraction : YES

Priority Encoder Extraction : Yes

Shift Register Extraction : YES

Logical Shifter Extraction : YES

XOR Collapsing : YES

ROM Style : Auto

Mux Extraction : Yes

Resource Sharing : YES

Asynchronous To Synchronous : NO

Use DSP Block : Auto

Automatic Register Balancing : No

---- Target Options

Add IO Buffers : YES

Global Maximum Fanout : 500

Add Generic Clock Buffer(BUFG) : 32

Number of Regional Clock Buffers : 48

Register Duplication : YES

Slice Packing : YES

Optimize Instantiated Primitives : NO

Use Clock Enable : Auto

Use Synchronous Set : Auto

Use Synchronous Reset : Auto

Pack IO Registers into IOBs : Auto

Equivalent register Removal : YES

---- General Options

Optimization Goal : Speed

Optimization Effort : 1

Power Reduction : NO

Keep Hierarchy : No

Netlist Hierarchy : As\_Optimized

RTL Output : Yes

Global Optimization : AllClockNets

Read Cores : YES

Write Timing Constraints : NO

Cross Clock Analysis : NO

Hierarchy Separator : /

Bus Delimiter : <>

Case Specifier : Maintain

Slice Utilization Ratio : 100

BRAM Utilization Ratio : 100

DSP48 Utilization Ratio : 100

Verilog 2001 : YES

Auto BRAM Packing : NO

Slice Utilization Ratio Delta : 5

=========================================================================

=========================================================================

\* HDL Compilation \*

=========================================================================

Compiling vhdl file "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Comb\_multiplier/ALEY\_MULTIPLIER.vhd" in Library work.

Entity <ALEY\_MULTIPLIER> compiled.

Entity <ALEY\_MULTIPLIER> (Architecture <MULTIPLIER\_arch>) compiled.

=========================================================================

\* Design Hierarchy Analysis \*

=========================================================================

Analyzing hierarchy for entity <ALEY\_MULTIPLIER> in library <work> (architecture <MULTIPLIER\_arch>) with generics.

WIDTH = 24

=========================================================================

\* HDL Analysis \*

=========================================================================

Analyzing generic Entity <ALEY\_MULTIPLIER> in library <work> (Architecture <MULTIPLIER\_arch>).

WIDTH = 24

Entity <ALEY\_MULTIPLIER> analyzed. Unit <ALEY\_MULTIPLIER> generated.

=========================================================================

\* HDL Synthesis \*

=========================================================================

Performing bidirectional port resolution...

Synthesizing Unit <ALEY\_MULTIPLIER>.

Related source file is "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Comb\_multiplier/ALEY\_MULTIPLIER.vhd".

WARNING:Xst:646 - Signal <S\_D<31:24>> is assigned but never used. This unconnected signal will be trimmed during the optimization process.

WARNING:Xst:643 - "C:/Users/Student/Desktop/BRYANT\_CSM/Bryant\_CSMSynthesis/Comb\_multiplier/ALEY\_MULTIPLIER.vhd" line 21: The result of a 24x24-bit multiplication is partially used. Only the 32 least significant bits are used. If you are doing this on purpose, you may safely ignore this warning. Otherwise, make sure you are not losing information, leading to unexpected circuit behavior.

Found 24x24-bit multiplier for signal <S\_D$mult0000> created at line 21.

Summary:

inferred 1 Multiplier(s).

Unit <ALEY\_MULTIPLIER> synthesized.

=========================================================================

HDL Synthesis Report

Macro Statistics

# Multipliers : 1

24x24-bit multiplier : 1

=========================================================================

=========================================================================

\* Advanced HDL Synthesis \*

=========================================================================

=========================================================================

Advanced HDL Synthesis Report

Macro Statistics

# Multipliers : 1

24x24-bit multiplier : 1

=========================================================================

=========================================================================

\* Low Level Synthesis \*

=========================================================================

WARNING:Xst:2677 - Node <Mmult\_S\_D\_mult00003> of sequential type is unconnected in block <ALEY\_MULTIPLIER>.

Optimizing unit <ALEY\_MULTIPLIER> ...

Mapping all equations...

Building and optimizing final netlist ...

Found area constraint ratio of 100 (+ 5) on block ALEY\_MULTIPLIER, actual ratio is 0.

Final Macro Processing ...

=========================================================================

Final Register Report

Found no macro

=========================================================================

=========================================================================

\* Partition Report \*

=========================================================================

Partition Implementation Status

-------------------------------

No Partitions were found in this design.

-------------------------------

=========================================================================

\* Final Report \*

=========================================================================

Final Results

RTL Top Level Output File Name : ALEY\_MULTIPLIER.ngr

Top Level Output File Name : ALEY\_MULTIPLIER

Output Format : NGC

Optimization Goal : Speed

Keep Hierarchy : No

Design Statistics

# IOs : 72

Cell Usage :

# BELS : 2

# GND : 1

# VCC : 1

# IO Buffers : 72

# IBUF : 48

# OBUF : 24

# DSPs : 3

# DSP48 : 3

=========================================================================

Device utilization summary:

---------------------------

Selected Device : 4vlx100ff1148-12

Number of Slices: 0 out of 49152 0%

Number of IOs: 72

Number of bonded IOBs: 72 out of 768 9%

Number of DSP48s: 3 out of 96 3%

---------------------------

Partition Resource Summary:

---------------------------

No Partitions were found in this design.

---------------------------

=========================================================================

TIMING REPORT

NOTE: THESE TIMING NUMBERS ARE ONLY A SYNTHESIS ESTIMATE.

FOR ACCURATE TIMING INFORMATION PLEASE REFER TO THE TRACE REPORT

GENERATED AFTER PLACE-and-ROUTE.

Clock Information:

------------------

No clock signals found in this design

Asynchronous Control Signals Information:

----------------------------------------

No asynchronous control signals found in this design

Timing Summary:

---------------

Speed Grade: -12

Minimum period: No path found

Minimum input arrival time before clock: No path found

Maximum output required time after clock: No path found

Maximum combinational path delay: 11.783ns

Timing Detail:

--------------

All values displayed in nanoseconds (ns)

=========================================================================

Timing constraint: Default path analysis

Total number of paths / destination ports: 555223 / 24

-------------------------------------------------------------------------

Delay: 11.783ns (Levels of Logic = 5)

Source: OP\_A<15> (PAD)

Destination: OP\_Q<23> (PAD)

Data Path: OP\_A<15> to OP\_Q<23>

Gate Net

Cell:in->out fanout Delay Delay Logical Name (Net Name)

---------------------------------------- ------------

IBUF:I->O 2 0.754 0.279 OP\_A\_15\_IBUF (OP\_A\_15\_IBUF)

DSP48:A15->PCOUT45 1 3.523 0.000 Mmult\_S\_D\_mult0000 (Mmult\_S\_D\_mult0000\_PCOUT\_to\_Mmult\_S\_D\_mult00001\_PCIN\_45)

DSP48:PCIN45->PCOUT34 1 1.890 0.000 Mmult\_S\_D\_mult00001 (Mmult\_S\_D\_mult00001\_PCOUT\_to\_Mmult\_S\_D\_mult00002\_PCIN\_34)

DSP48:PCIN34->P5 1 1.816 0.266 Mmult\_S\_D\_mult00002 (OP\_Q\_22\_OBUF)

OBUF:I->O 3.255 OP\_Q\_22\_OBUF (OP\_Q<22>)

----------------------------------------

Total 11.783ns (11.238ns logic, 0.545ns route)

(95.4% logic, 4.6% route)

=========================================================================

Total REAL time to Xst completion: 5.00 secs

Total CPU time to Xst completion: 4.44 secs

-->

Total memory usage is 4554220 kilobytes

Number of errors : 0 ( 0 filtered)

Number of warnings : 3 ( 0 filtered)

Number of infos : 0 ( 0 filtered)